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Defensive Loop Tiling for Multi-core Processors

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New Challenges in Multi-core Era

- Some levels of caches are shared by cores
- Different programs can compete for cache
- The available cache size is a run-time information
  - A wrong selection of tile sizes can forfeit the benefit of tiling

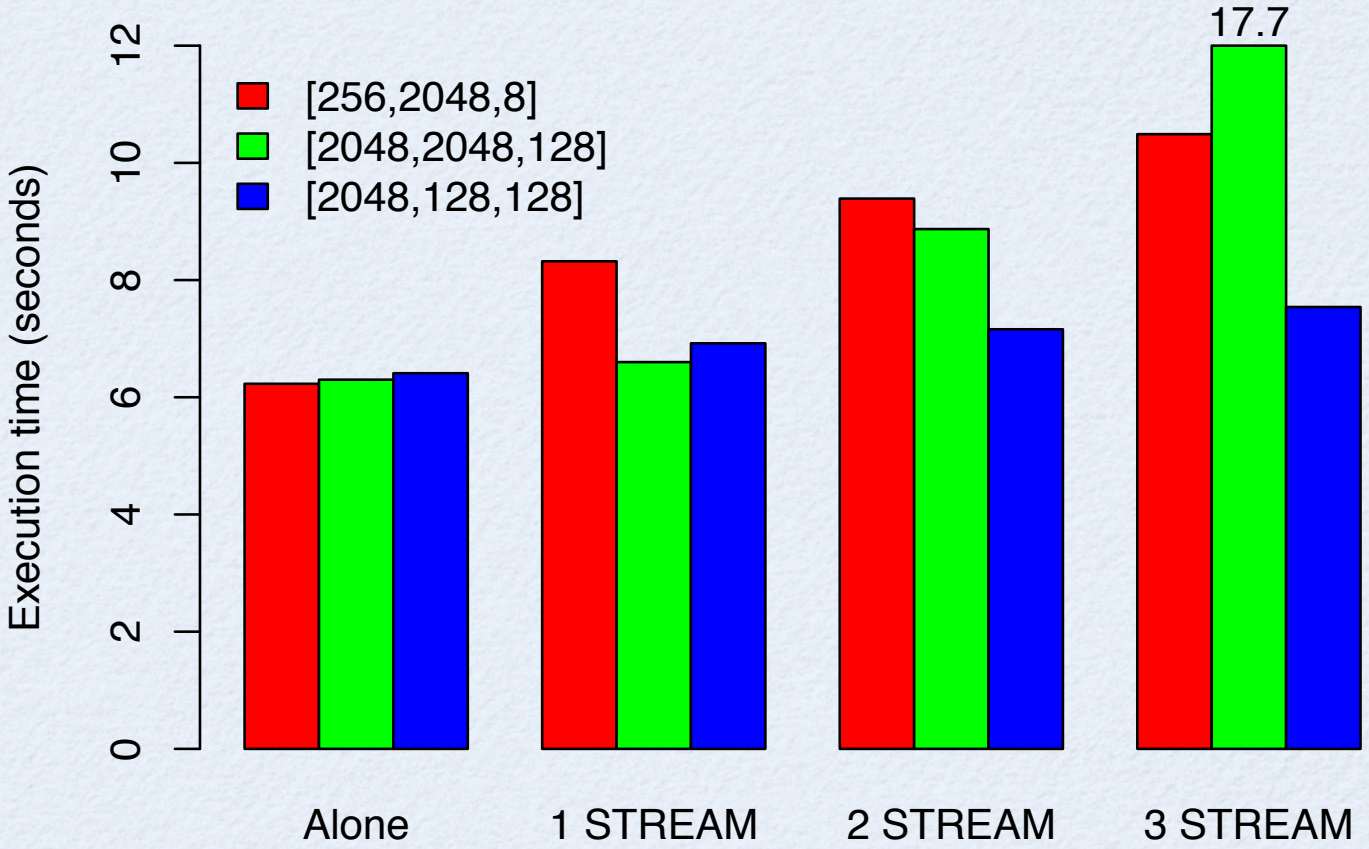
Reuse Distance Analysis

- Cache configuration
  - L1: 32KB, private
  - L2: 256KB, private
  - L3: 8MB, shared
- Reuse distance

Loop level	Reuse data	[256,2048,8]	[2048,2048,128]	[2048,128,128]
k	C[i][j]	32KB	32KB	2KB
i	B[k][j]	144KB	2065KB	130KB
kk	C[i][j]	4240KB	36MB	4224KB

Performance Comparison

- Matrix multiplication co-run with up to 3 STREAM benchmarks
- Search all the power of 2 tiling factors, [TI,TJ,TK]



Discussion

- Model cache interference as a function of tile size
- Balance the performance for different co-run environments
- Distinguish inclusive cache and non-inclusive cache
- Combine with prefetching effect